Digital And power electronics

LAB MANUAL

3rd SEMESTER

B.Voc Automotive Mechatronics

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Experiment No. – 1

AIM: To study the operation of single phase fully controlled converter using R and RL load and to observe the output waveforms.

Apparatus Required:

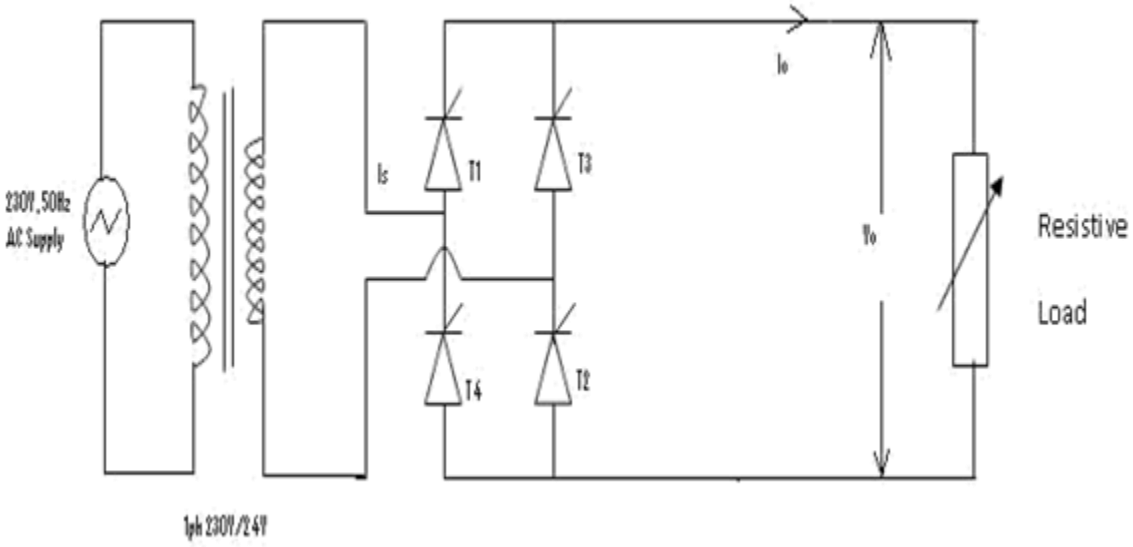
1. Power thyristors
2. Rheostat
3. CRO
4. Transformer (1-phase) 230V/24V
5. Connection wires

Theory:

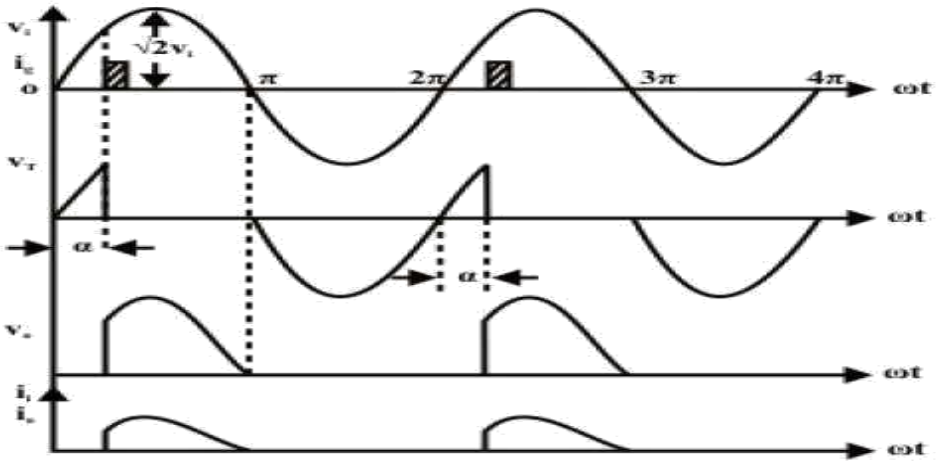
A fully controlled converter or full converter uses thyristors only and there is a wider control over the level of dc output voltage. With pure resistive load, it is single quadrant converter. Here, both the output voltage and output current are positive. With RL- load it becomes a two-quadrant converter. Here, output voltage is either positive or negative but output current is always positive. Figure shows the quadrant operation of fully controlled bridge rectifier with R-load. Fig shows single phase fully controlled rectifier with resistive load. This type of full wave rectifier circuit consists of four SCRs. During the positive half cycle, SCRs T1 and T2 are forward biased. At $\omega t = \alpha$, SCRs T1 and T3 are triggered, then the current flows through the L – T1- R load – T3 – N. At $\omega t = \pi$, supply voltage falls to zero and the current also goes to zero. Hence SCRs T1 and T3 turned off. During negative half cycle (π to 2π). SCRs T3 and T4 forward biased. At $\omega t = \pi + \alpha$, SCRs T2 and T4 are triggered, then current flows through the path N – T2 – R load- T4 – L. At $\omega t = 2\pi$, supply voltage and current goes to zero, SCRs T2 and T4 are turned off. The Fig-3, shows the current and voltage waveforms for this circuit. For large power dc loads, 3-phase ac to dc converters are commonly used. The various types of three-phase phase-controlled converters are 3 phase half-wave converter, 3-phase semi converter, 3-phase full controlled and 3-phase dual converter. Three-phase half-wave converter is rarely used in industry because it introduces dc component in the supply current. Semi converters and full converters are quite common in industrial applications. A dual is used only when reversible dc drives with power ratings of several MW are required. The advantages of three phase converters over single-phase converters are as under: In 3-phase converters, the ripple frequency of the converter output voltage is higher than in single-phase converter. Consequently, the filtering requirements for smoothing out the load current are less. The

load current is mostly continuous in 3-phase converters. The load performance, when 3- phase converters are used, is therefore superior as compared to when single-phase converters are used.

Vout=(2Vs)(Cosα)/π **Iavg=Vavg/R**



Circuit Diagram



Model Graph

Observation Table:

Serial No.	Triggering angle 'α' degree	Output voltage Voav (volt) (measured)	Time period(ms)
1 2 3			

Procedure:

1. Single Phase Fully Controlled Bridge Rectifier
2. Make the connections as per the circuit diagram.
3. Connect CRO and multimeter (in dc) across the load.
4. Keep the potentiometer (Ramp control) at the minimum position (maximum resistance).
5. Switch on the step-down ac source.
6. Check the gate pulses at G1-K1, G2-K2, G3-K3, & G4-K4 respectively.
7. Observe the waveform on CRO and note the triggering angle 'α' and note the corresponding reading of the multimeter. Also note the value of maximum amplitude Vm from the waveform.
8. Set the potentiometer at different positions and follow the step given in (6) for every position.
9. Tabulate the readings in observation column.
10. Draw the waveforms observed on CRO.

Result:

Thus, the operation of single phase fully controlled converter using R and RL load has been studied and the output waveforms has been observed.

Experiment No. – 2

AIM: To draw the characteristics of DIAC.

APPARATUS REQUIRED:

S.No	Name	Range	Qty
1.	Regulated power supply (R.P.S)	(0-30) V (0-300) V	1
2.	Ammeter	(0-50) mA (0-30) mA (0-10) mA	1
3.	Voltmeter	(0-50) V (0-15) V	1.

COMPONENTS REQUIRED:

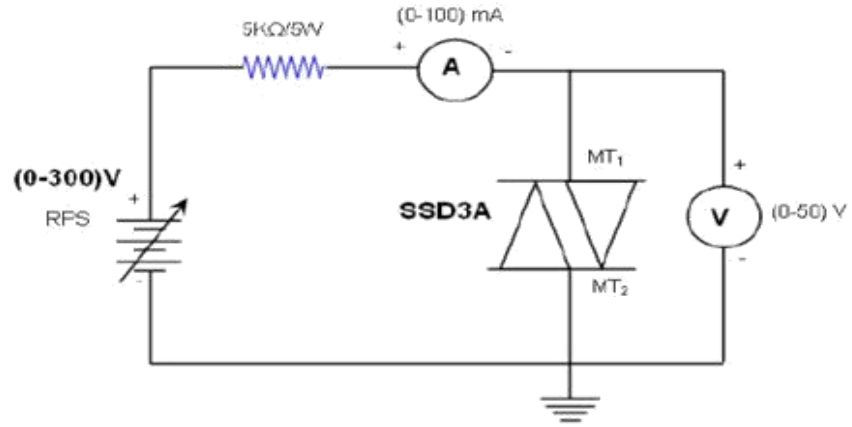
S.No	Name	Range	Qty
1.	DIAC	3 A	1
2.	Resistor	5K Ω, 1K Ω	1
3.	Bread Board		1
4.	Wires		As per Requirement.

Theory: A DIAC is a two terminal three-layer bidirectional device which can be switched from its off state to on state for either polarity of applied voltage. The operation of DIAC is identical both in forward and reverse conduction. T he DIAC does not conduct until the applied voltage of either polarity the break over voltage VBO.

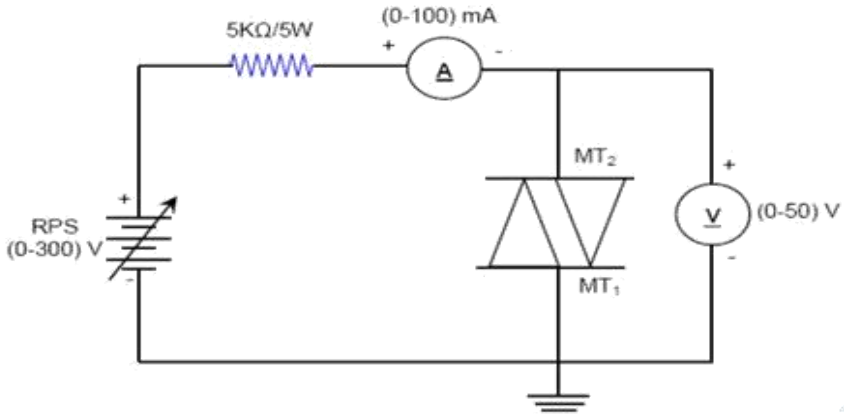
Characteristics of Diac:

Circuit Diagram:

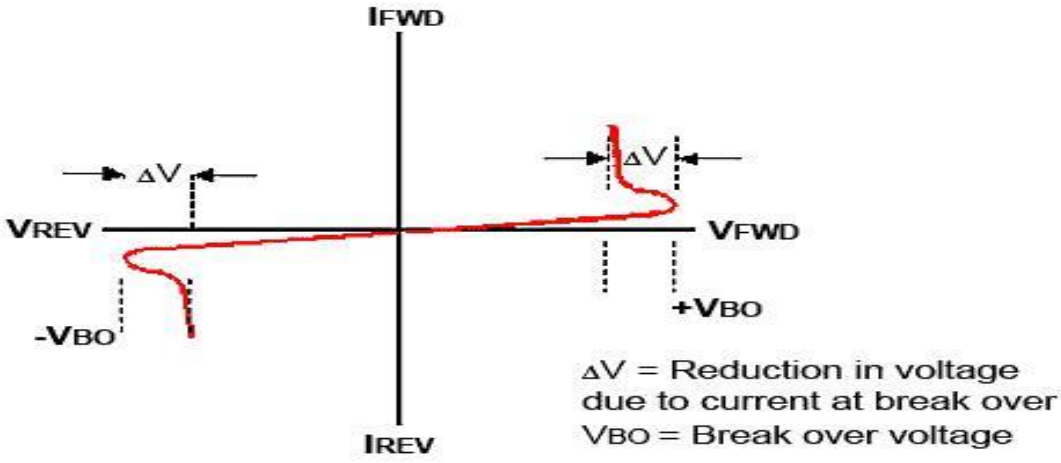
Forward Direction:



Reverse Direction:



Model Graph



Procedure:

- The connections are made as shown in the circuit diagram.
- First DIAC is connected in forward direction
- The input supply is increased in step by step by varying the RPS
- The corresponding ammeter and voltmeter readings are noted and tabulated.
- Then the DIAC is connected in reverse condition.
- The above process is repeated.

Tabulation:

S.NO	Forward direction		Reverse direction	
	Voltage (volts)	Current (ma)	Voltage (volts)	Current (ma)

Result:

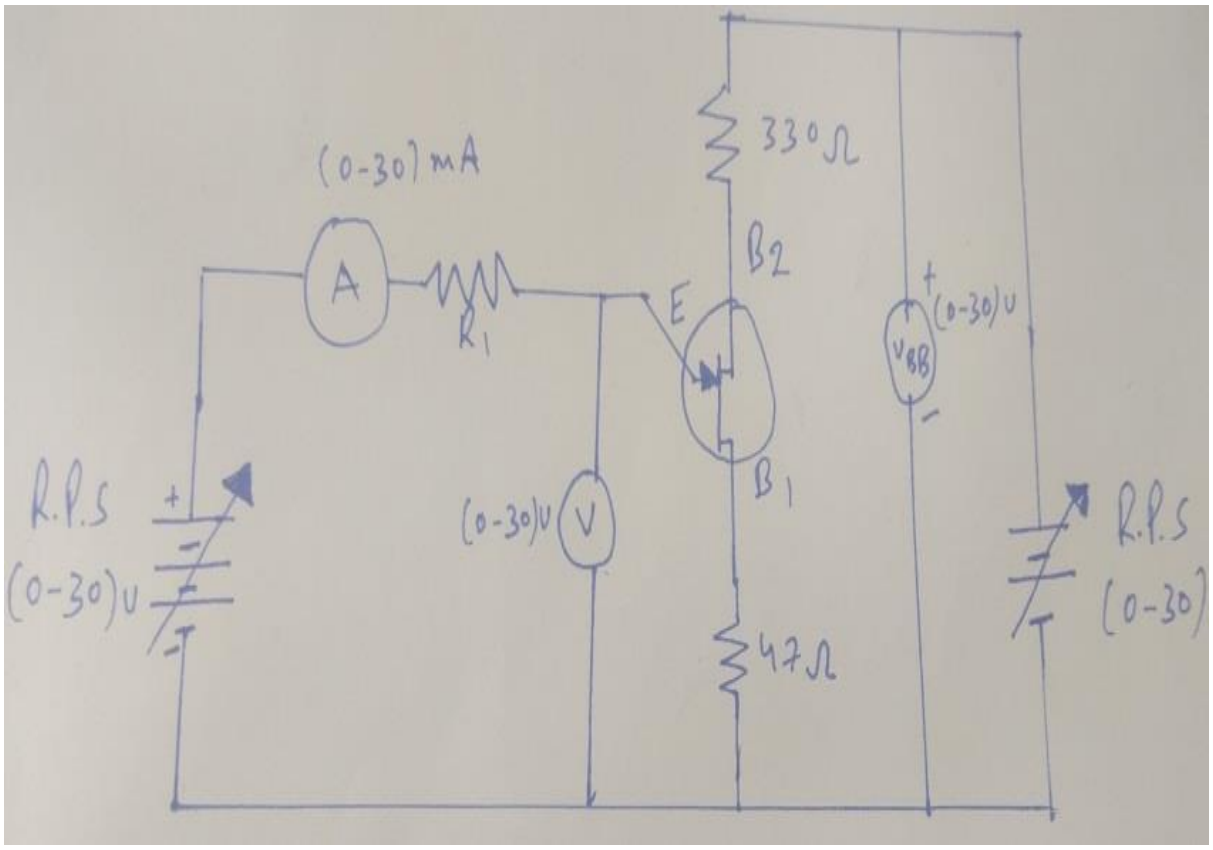
Thus, the V-I characteristics of DIAC was obtained and graph was drawn.

Experiment No. – 3

AIM: To draw the characteristics of Uni Junction Transistor (UJT).

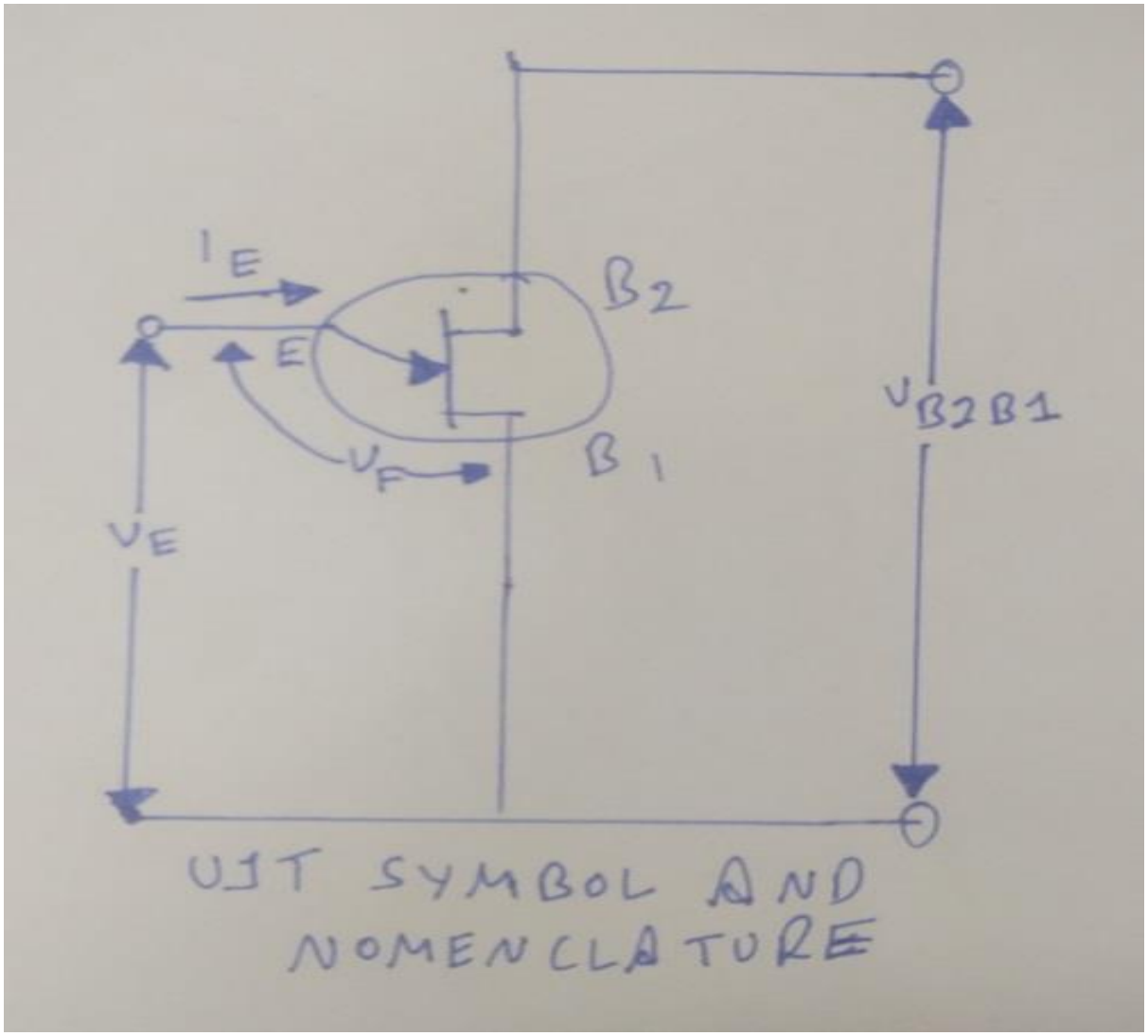
APPARATUS REQUIRED: Regulated Power Supply (2Nos) (0-30V, 1A), UJT 2N2646, Resistors 10kΩ, 47Ω, 330Ω, Multimeters, Breadboard and Connecting Wires.

CIRCUIT DIAGRAM:



THEORY:

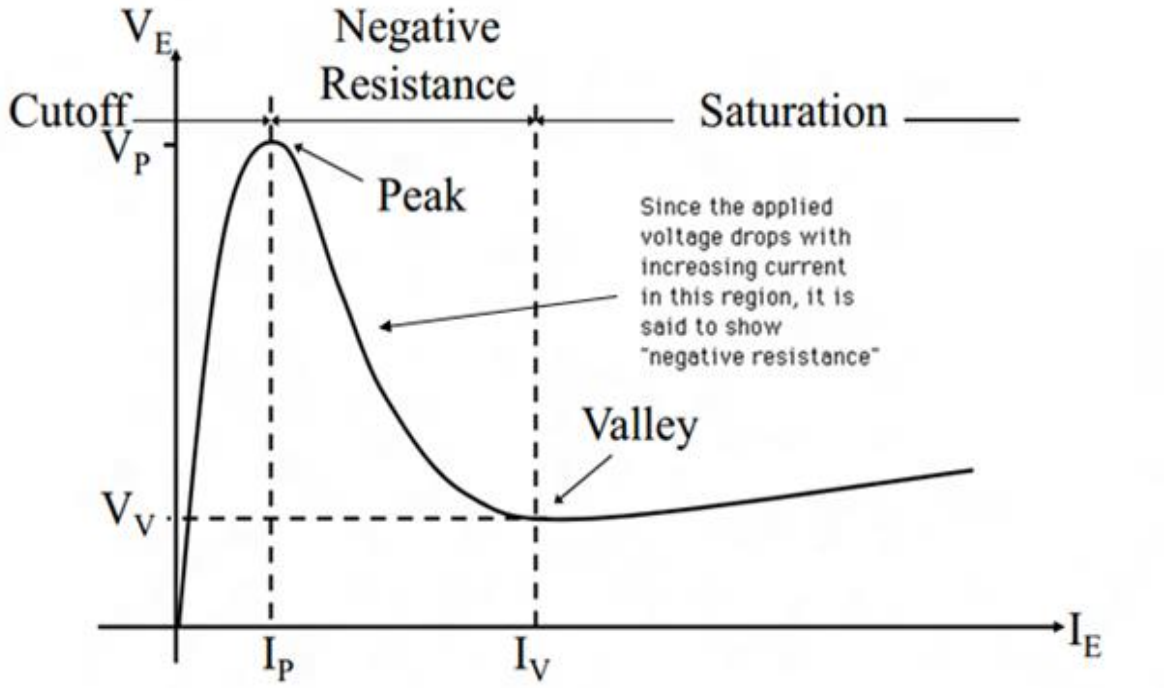
A Unijunction Transistor (UJT) is an electronic semiconductor device that has only one junction. It has three terminals an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called interbase resistance. The original UJT, is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length.



The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect is a negative resistance at the emitter terminal.

This is what makes the UJT useful, especially in simple oscillator circuits. When the emitter voltage reaches V_p, the current starts to increase and the emitter voltage starts to decrease. This is represented by negative slope of the characteristics which is referred to as the negative resistance region, beyond the valley point, V_{EB} proportional to I_E.

CHARACTERISTICS CURVE:



PROCEDURE:

1. Connection is made as per circuit diagram.

2. Output voltage is fixed at a constant level and by varying input voltage corresponding emitter current values are noted down.

3. This procedure is repeated for different values of output voltages.
4. All the readings are tabulated and Intrinsic Stand-Off ratio is calculated using
   $\eta = (V_p - V_D) / V_{B2B1}$
5. A graph is plotted between V_E and I_E for different values of V_{B2B1}.

OBSERVATIONS:

V_{B2B1}=2V		**V_{B2B1}=3V**	
V_{EB}(V)	**I_E(mA)**	**V_{EB}(V)**	**I_E(mA)**

CALCULATIONS:

$$VP = \eta VB2B1 + VD$$

$$\eta = (V_P - V_D) / V_{B2B1}$$

$$\eta = (\eta_1 + \eta_2) / 2$$

APPLICATION: UJT can be used as trigger device for SCR's. traic and other applications including sawtooth generator, phase control and timing circuits.

Experiment No. – 4

AIM: To construct a UJT relaxation oscillator and plot the wave forms at emitter, base1 and base2

EQUIPMENTS / COMPONENTS

Sl. no.	Name and Specification		Quantity
1.	Resistors	100 Ω 10 KΩ	2 nos. 1 no.
2.	Capacitor	0.1 µF	1 no.
3.	UJT	2N2646	1 no.
4.	Power supply	10 V DC	1 no.
5.	Oscilloscope	0 to 20 MHz	1 no.
6.	Multimeter		1 no.
7.	Breadboard		1 no.
8.	Connecting wires		

PRINCIPLE

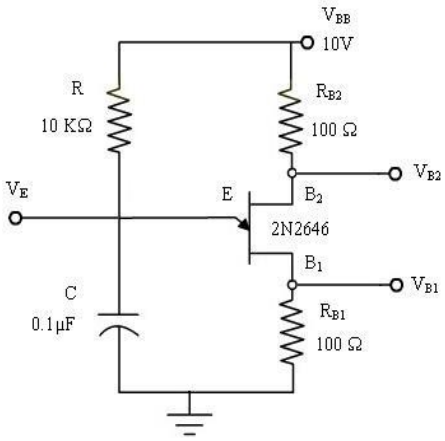
UJT is a unipolar device. It is constructed using an N type silicon bar on which a P type silicon material is doped. It has three terminals namely base1 (B_1), base2 (B_2) and emitter (E). The RC circuit associated with UJT will function as a relaxation oscillator. The sharp pulse available from the circuit can be used as trigger pulse for various applications.

Once the power supply is switched ON, Capacitor C charges through R towards V_{BB}. Then the voltage across the capacitor reaches V_p (= ηV_{BB}+ V_d), where η = 0.63, V_d = 0.7V, UJT turns ON and it enters a negative resistance region. The capacitor rapidly discharges through UJT, since it then offers very low resistance. This sudden discharge develops a sharp pulse at B_1. When the capacitor voltage reaches valley voltage (V_v) of UJT it turns OFF. This enables the capacitor to charge again and repeat the cycle.

PROCEDURE

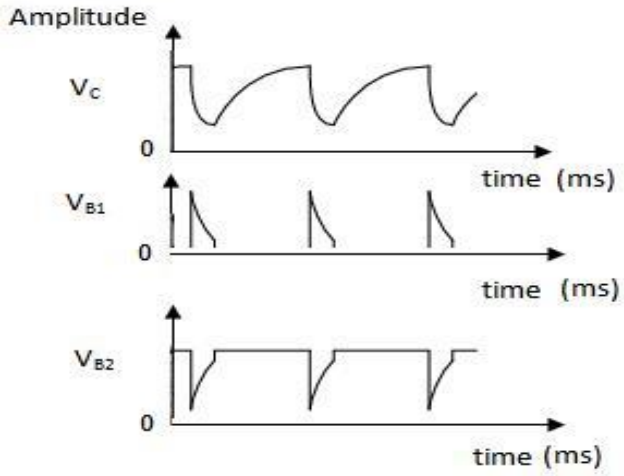
1. Check the given components
2. Understand the pins of UJT
3. Assemble the circuit in a bred board
4. Connect the output of the circuit to an oscilloscope
5. Switch ON the power supply
6. Observe the wave forms at V_E,V_{B1},V_{B2}
7. Measure the amplitude and time periods.
8. Plot waveforms.

CIRCUIT DIAGRAM



OBSERVATIONS

Waveforms



Experiment No. – 5

AIM: Configuring NAND and NOR logic gates as universal gates.

NAND gate as a universal gate

Apparatus: logic trainer kit, NAND gates (IC 7400), wires.

Theory:

NAND gate is actually a combination of two logic gates: AND gate followed by NOT gate. So its output is complement of the output of an AND gate.

This gate can have minimum two inputs, output is always one. By using only NAND gates, we can realize all logic functions: AND, OR, NOT, X-OR, X-NOR, NOR. So this gate is also called universal gate.

NAND gates as NOT gate

A NOT produces complement of the input. It can have only one input, tie the inputs of a NAND gate together. Now it will work as a NOT gate. Its output is

$$Y = (A.A)'$$

$$\Rightarrow \quad Y = (A)'$$

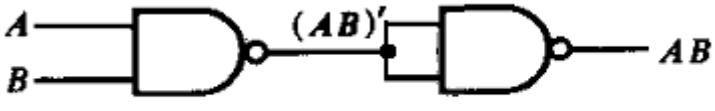
NOT (inverter)

NAND gates as AND gate

A NAND produces complement of AND gate. So, if the output of a NAND gate is inverted, overall output will be that of an AND gate.

$$Y = ((A.B)')'$$

$$\Rightarrow \quad Y = (A.B)$$



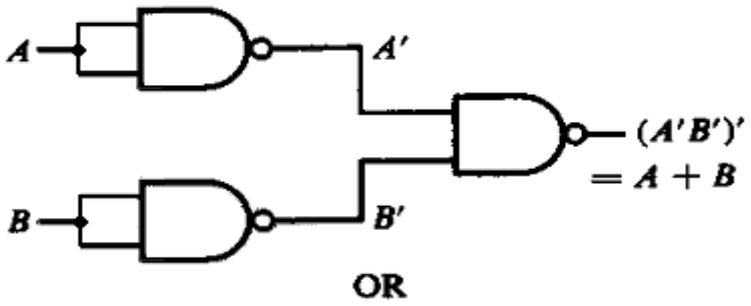
AND

NAND gates as OR gate

From DeMorgan's theorems: $(A.B)' = A' + B'$

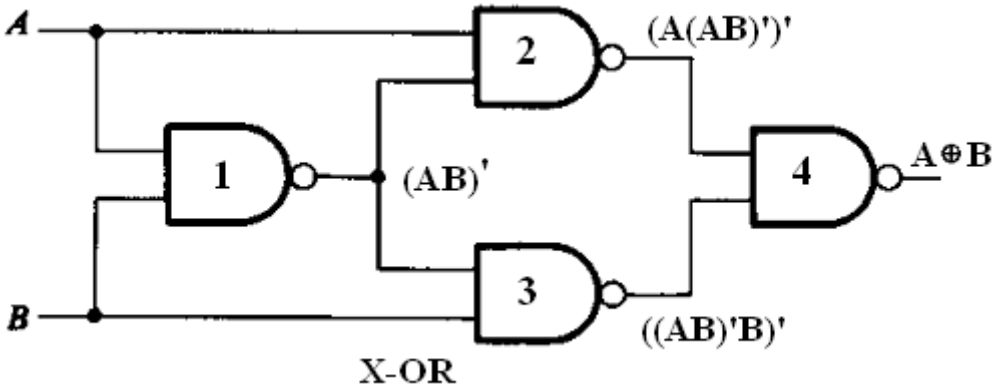
$$\Rightarrow \quad (A'.B')' = A'' + B'' = A + B$$

So, give the inverted inputs to a NAND gate, obtain OR operation at output.



NAND gates as X-OR gate

The output of a to input X-OR gate is shown by: Y = A'B + AB'. This can be achieved with the logic diagram shown in the left side.



Gate No.	Inputs	Output
1	A, B	(AB)'
2	A, (AB)'	(A (AB)')'
3	(AB)', B	(B (AB)')'
4	(A (AB)')', (B (AB)')'	A'B + AB'

Now the output from gate no. 4 is the overall output of the configuration.

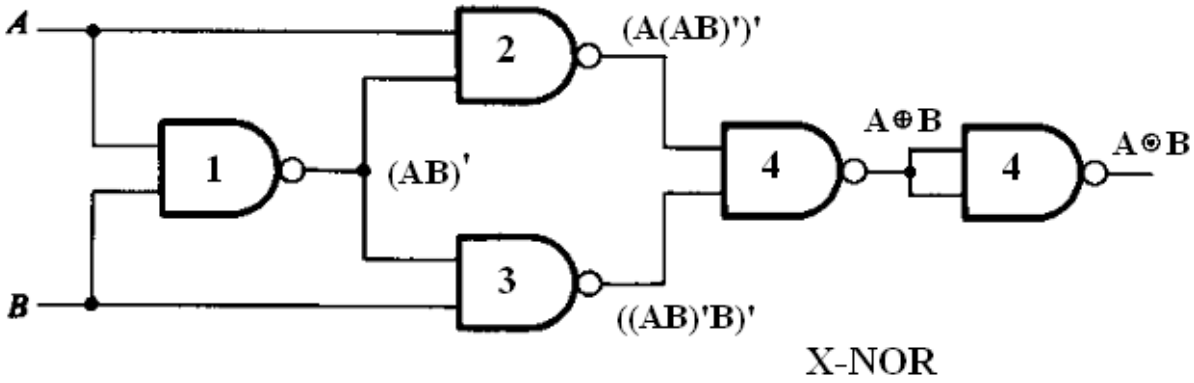
Y = ((A (AB)')' (B (AB)')')'
= (A(AB)')'' + (B(AB)')''
= (A(AB)') + (B(AB)')
= (A(A' + B)') + (B(A' + B'))
= (AA' + AB') + (BA' + BB')
= (0 + AB' + BA' + 0)
= AB' + BA'

=> Y = AB' + A'B

NAND gates as X-NOR gate

X-NOR gate is actually X-OR gate followed by NOT gate. So give the output of X-OR gate to a NOT gate, overall output is that of an X-NOR gate.

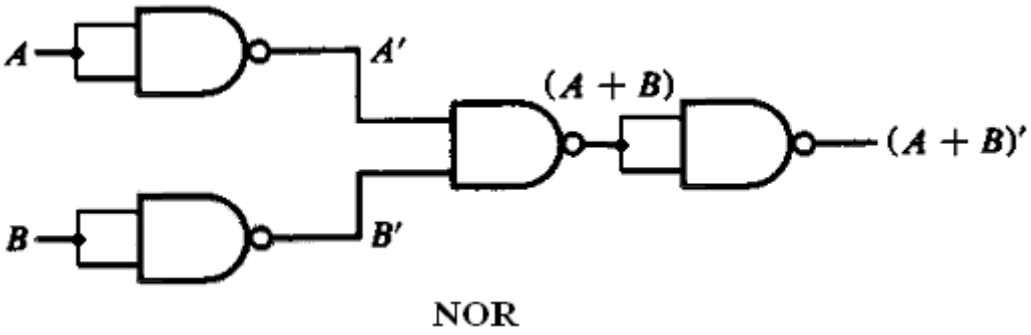
Y = AB+ A'B'



NAND gates as NOR gate

A NOR gate is an OR gate followed by NOT gate. So connect the output of OR gate to a NOT gate, overall output is that of a NOR gate.

Y = (A + B)'



Procedure:

1. Connect the trainer kit to ac power supply.
2. Connect the NAND gates for any of the logic functions to be realised.
3. Connect the inputs of first stage to logic sources and output of the last gate to logic indicator.
4. Apply various input combinations and observe output for each one.
5. Verify the truth table for each input/ output combination.
6. Repeat the process for all logic functions.
7. Switch off the ac power supply.

NOR gate as a universal gate

Apparatus: logic trainer kit, NOR gates (IC 7402), wires.

Theory:

NOR gate is actually a combination of two logic gates: OR gate followed by NOT gate. So its output is complement of the output of an OR gate.

This gate can have minimum two inputs, output is always one. By using only NOR gates, we can realize all logic functions: AND, OR, NOT, X-OR, X-NOR, NAND. So this gate is also called universal gate.

NOR gates as NOT gate

A NOT produces complement of the input. It can have only one input, tie the inputs of a NOR gate together. Now it will work as a NOT gate. Its output is

Y = (A+A)'

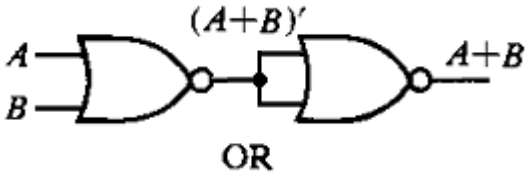
=> Y = (A)'

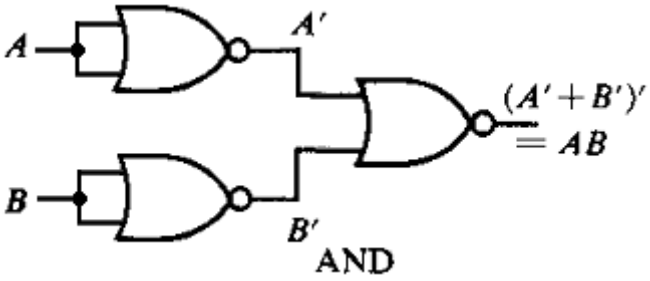
NOR gates as OR gate

A NOR produces complement of OR gate. So, if the output of a NOR gate is inverted, overall output will be that of an OR gate.

Y = ((A+B)')'

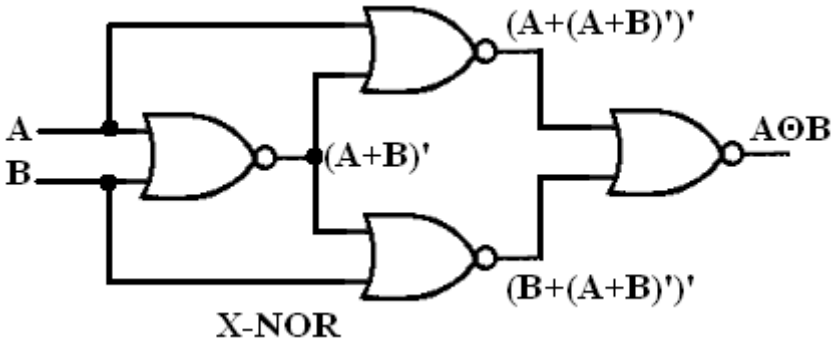
=> Y = (A+B)





NOR gates as AND gate

From DeMorgan's theorems: (A+B)' = A'B'
=> (A'+B')' = A''B'' = AB
So, give the inverted inputs to a NOR gate, obtain AND operation at output.



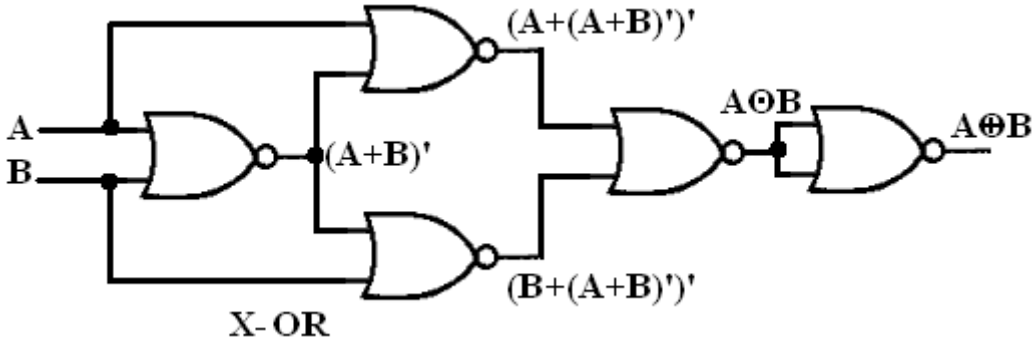
NOR gates as X-NOR gate

The output of a two input X-NOR gate is shown by: Y = AB + A'B'. This can be achieved with the logic diagram shown in the left side.

Gate No.	**Inputs**	**Output**
1	A, B	(A + B)'
2	A, (A + B)'	(A + (A+B)')'
3	(A + B)', B	(B + (A+B)')'
4	(A + (A + B)')', (B + (A+B)')'	AB + A'B'

Now the output from gate no. 4is the overall output of the configuration.

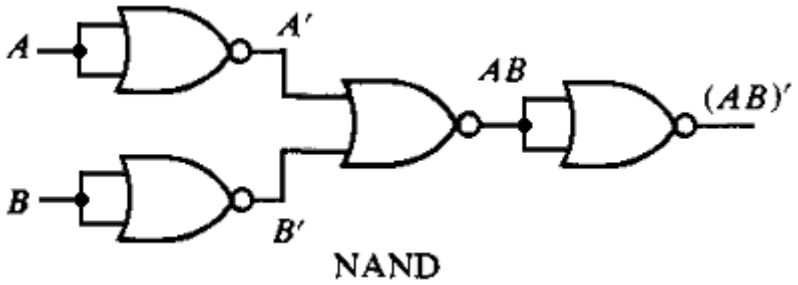
Y = ((A + (A+B)')' (B +(A+B)')')'
= (A+(A+B)'')''.(B+(A+B)')''
= (A+(A+B)').(B+(A+B)')
= (A+A'B').(B+A'B')
= (A + A').(A + B').(B+A')(B+B')
= 1.(A+B').(B+A').1
= (A+B').(B+A')
= A.(B + A') +B'.(B+A')
= AB + AA' +B'B+B'A'
= AB + 0 + 0 + B'A'
= AB + B'A'
=> Y = AB + A'B'



NOR gates as X-OR gate

X-OR gate is actually X-NOR gate followed by NOT gate. So give the output of X-NOR gate to a NOT gate, overall output is that of an X-OR gate.

$$Y = A'B + AB'$$



NOR gates as NAND gate

A NAND gate is an AND gate followed by NOT gate. So, connect the output of AND gate to a NOT gate, overall output is that of a NAND gate.

$$Y = (AB)'$$

Procedure:

1. Connect the trainer kit to ac power supply.
2. Connect the NOR gates for any of the logic functions to be realised.
3. Connect the inputs of first stage to logic sources and output of the last gate to logic indicator.
4. Apply various input combinations and observe output for each one.
5. Verify the truth table for each input/ output combination.
6. Repeat the process for all logic functions.
7. Switch off the ac power supply.

Experiment No. – 6

AIM: Implementation of the given Boolean function using logic gates in both SOP and POS forms.

APPARATUS REQUIRED:

S.No.	Name of apparatus	Specification	Quantity
1	SOP & POS kit	Using 7404,7408, 7432.	01
2	Patch cords	----------	As required

THEORY:

Logical functions are generally expressed in terms of logical variables. Values taken on by the logical functions and logical variables are in the binary form. An arbitrary logic function can be expressed in the following forms:

(i) Sum of Products (SOP)
(ii) Product of Sums (POS**)**

Sum of Products (SOP):

The logic sum of two or more logical product terms is called a *Sum of Products* expression. It is basically an OR operation of AND operated variable such as:

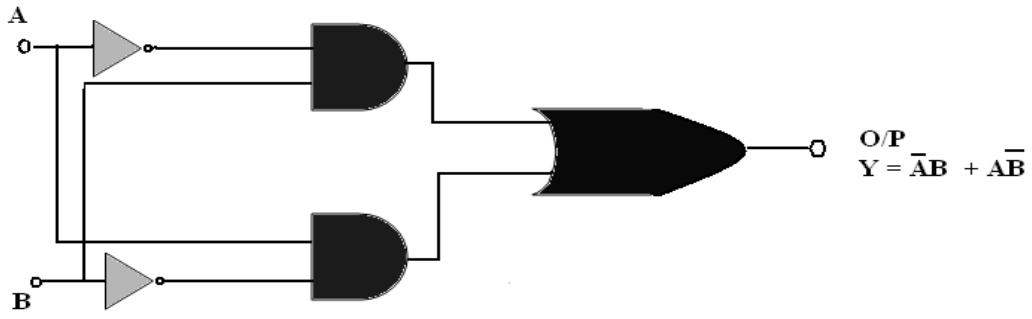
Y = AB + BC + AC

Y = AB + $\overline{A}$C + BC

In this approach we simplified the given Boolean expression using basic Boolean lows and theorem. In this approach we assign 1 value to normal variable and 0 to its complements.

Also considered the values to find the expression from any arithmetic or logic calculation.

Sum of Product solution logic diagram



Product of Sum (POS)

Product of Sums (POS):

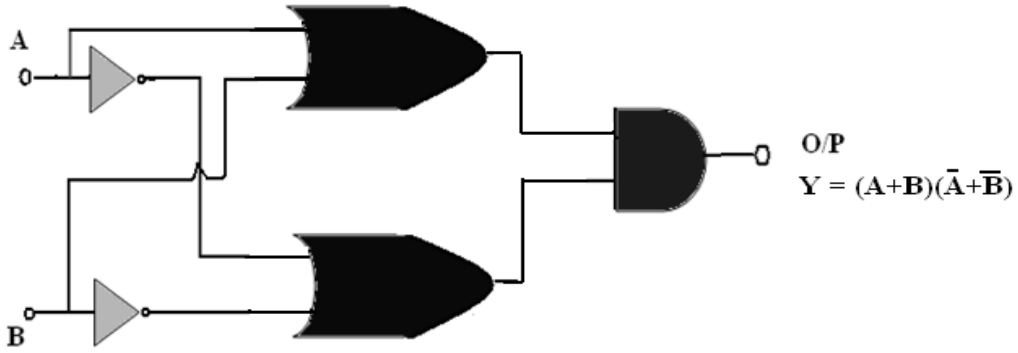
A product of sums expression is a logical product of two or more logical sum terms. It is basically an AND operation of OR operated variables such as:

(i) Y = (A+B) (B+C)(C+$\bar{A}$)
(ii) Y = (A+B+C)(A+ $\bar{C}$)

In POS form we simplified the given Boolean expression using basic Boolean lows and theorem. In this approach we assign 0 values to normal variable and 1 to its complements.

Also considered the values to find the expression from any arithmetic or logic calculation.

The POS solution logic diagram



Procedure: -

- Connect the circuit as per circuit diagram.
- Switch ON the experimental board.
- Give the inputs to A & B through switches.
- Switch ON the experimental board.
- Observed the output y on the kit through LEDs
- For different combination of inputs observe the output and match them with respective truth table and verify the equations SOP & POS.

INPUT		OUTPUT
A	B	Y=$(\bar{A}+B)(A+\bar{B})$
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table for POS

Truth Table for SOP

INPUT		OUTPUT
A	B	Y=$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

RESULT:

Study of Boolean function and both equations SOP&POS are verified.

PRECAUTIONS:

- All the ICs should be checked before starting the experiment.
- All the connection should be tight.
- Always connect ground 1st and then connect Vcc.
- Suitable type wire should be used for different types of circuit.
- The kit should be Off before change the connections.
- After completed the experiment switched off the supply of the apparatus.

Experiment No. – 7

AIM: To realize Half Adder and Full Adder using Basic gates.

APPARATUS REQUIRED:

IC 7408, IC 7486, IC 7432, Patch Cords & IC Trainer Kit.

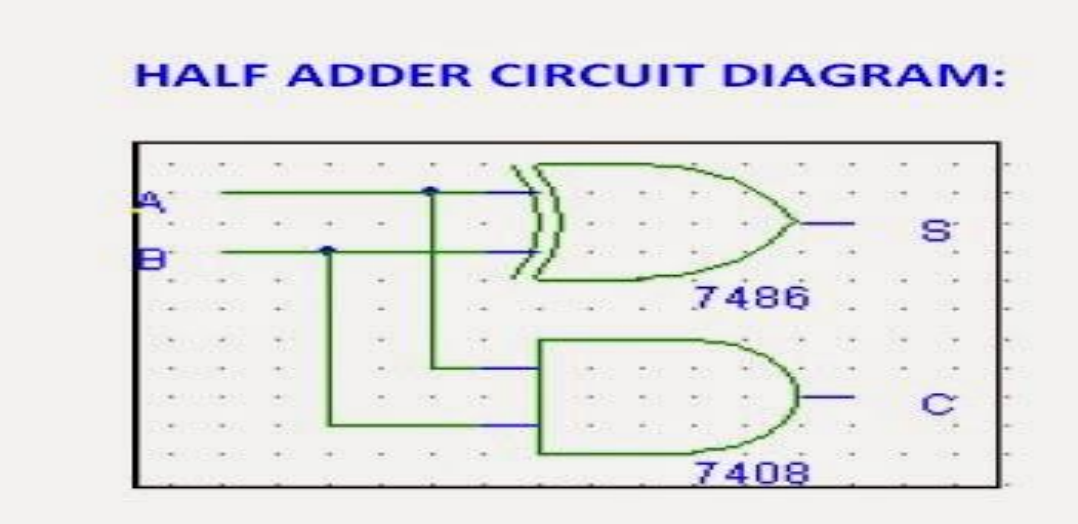
THEORY:

Adder circuit is a combinational digital circuit that is used for adding two numbers. A typical adder circuit produces a sum bit (denoted by S) and a carry bit (denoted by C) as the output. Typically, adders are realized for adding binary numbers but they can be also realized for adding other formats like BCD (binary coded decimal, XS-3 etc. Besides addition, adder circuits can be used for a lot of other applications in digital electronics like address decoding, table index calculation etc. Adder circuits are of two types: Half adder ad Full adder.

Half-Adder: A combinational logic circuit that performs the addition of two data bits, A and
B, is called a half-adder. Addition will result in two output bits; one of which is the sum bit, S, and the other is the carry bit, C. The Boolean functions describing the half-adder are: S =A Å B C = A B

Full-Adder: The half-adder does not take the carry bit from its previous stage into account. This carry bit from its previous stage is called carry-in bit. A combinational logic circuit that adds two data bits, A and B, and a carry-in bit, Cin , is called a full-adder. The Boolean functions describing the full-adder are:
S = (x Å y) Å Cin C = xy + Cin (x Å y)

Half adder circuit diagram:



TRUTH TABLE

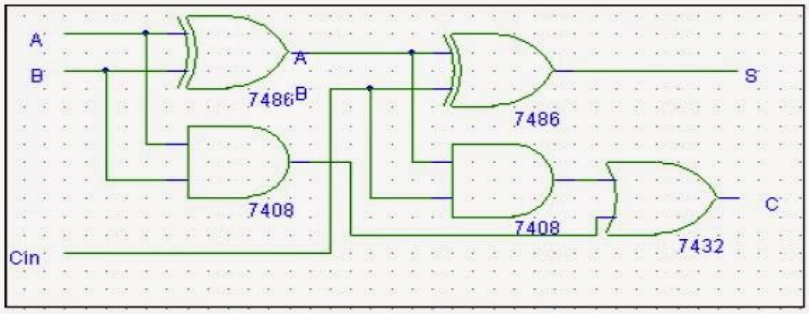
INPUTS		OUTPUTS	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

BOOLEAN EXPRESSIONS:

$$S = A \oplus B$$
$$C = A\ B$$

Full adder circuit diagram:

FULL ADDER CIRCUIT DIAGRAM :



FULL ADDER TRUTH TABLE

INPUTS			OUTPUTS	
A	B	Cin	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

BOOLEAN EXPRESSIONS:

$$S = A \oplus B \oplus C$$

$$C = A\,B + B\,Cin + A\,Cin$$

Procedure:

- Check the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

Precautions:

- All IC's must be checked before start the experiment.
- All connections should made and tight.
- While making connections main voltage should be kept switch off.
- The circuit should be OFF before change the connection.

Experiment No. – 8

AIM: Verification of state tables of R-S flip-flop, J - K flip-flop, T Flip-Flop, D Flip-Flop Using NAND and NOR gates.

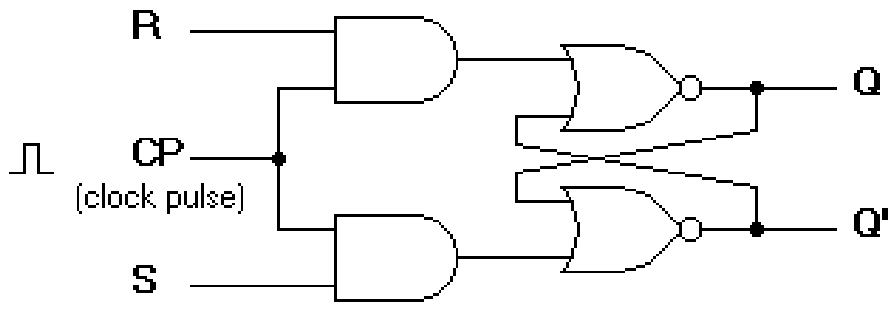
Apparatus: - IC 7400 (NAND Gate), IC 7402 (NOR Gate), IC 7408 (AND Gate).

Theory: -

In case of sequential circuits, the effect of all previous inputs on the outputs is represented by a state of the circuit. Thus, the output of the circuit at any time depends upon its current state and the input. These also determine the next state of the circuit. The relationship that exists among the inputs, outputs, present and next states can be specified by either the state table or the state diagram. State Table: - The state table representation of a sequential circuit consists of three sections labelled present state next state and output. The present state designates the state of flip – flops before the occurrence of a clock pulse. The next state shows the states of flip - flops after the clock pulse, and the output section lists the value of the output variables during the present state.

Flip-Flop: -The basic one-bit digital memory circuit is known as flip-flop. It can store either 0 or 1. Flip-flops are classifieds according to the number of inputs.

R-S Flip-Flop: - The circuit is similar to SR latch except enable signal is replaced by clock pulse.



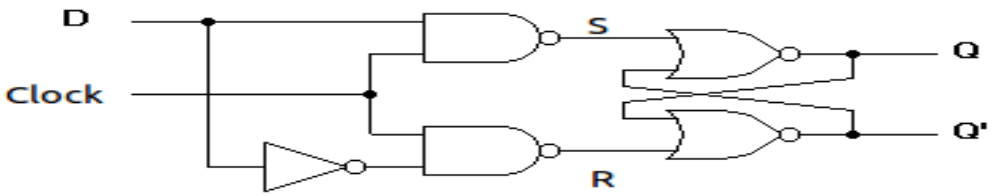
R-S Flip-Flop

Truth Table:

CLOCK PULSE	S	R	Q(T+1)
0	X	X	QT
1	0	0	QT
1	1	0	SET
1	0	1	RESET
1	1	1	INDETERMINATE?

D Flip-Flop: -

A D FF has a single data input. This type of FF is obtained from the SR FF by connecting the R input through an inverter, and the S input is connected directly to data input. The modified clocked SR flip-flop is known as D-flip-flop and is shown below. From the truth table of SR flip-flop, we see that the output of the SR flip-flop is in unpredictable state when the inputs are same and high. In many practical applications, these input conditions are not required. These input conditions can be avoided by making then complement of each other.
Logic Diagram:



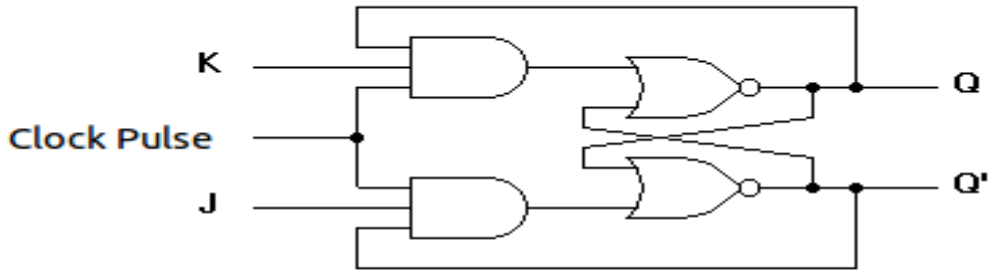
D-Flip Flop

Characteristic table for D flip flop

Clock Pulse	D input	Q(t+1)
0	x	0
1	0	0
1	1	1

J-K Flip-Flop: - In a RS flip-flop the input R=S=1 lead to an indeterminate output. The RS flip-flop circuit may be re-joined if both inputs are 1 than also
The complementary of each other.

Diagram

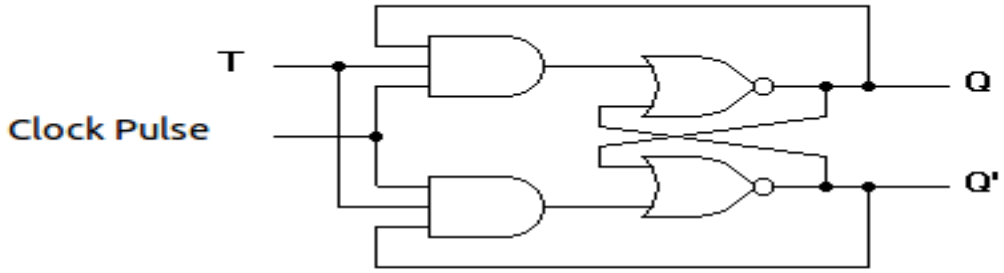


J-K flip Flop

Characteristic table for J-K flip flop

Clock Pulse	J	K	Q(t+1)
0	x	x	NC
1	0	0	NC
1	0	1	Reset
1	1	0	Set
1	1	1	Togle (Qt)'

T Flip-Flop: - T flip-flop is known as toggle flip-flop. The T flip-flop is modification of the J-K flip-flop. Both the JK inputs of the JK flip – flop is held at logic 1 and the clock signal continuous to change.



T-Flip Flop

Clock Pulse	T Input	Q(t+1)
0	x	NC
1	0	NC
1	1	Toggle (Qt)'

Procedure: -

- Connections are made as per circuit diagram.
- Verify truth- tables for various combinations of input.

RESULT: -

- Study and verified truth-tables of various flip-flops.

Precaution: -

1. All the IC's should be checked before use the apparatus.
2. All LED's should be checked.
3. All connections should be tight.
4. Always connect GROUND first and then Vcc
5. The circuit should be off before change the connections.
6. After completing the experiment switch off the supply to apparatus.

Experiment No. – 9

AIM: Implementation & verification of Decoder/Demultiplexer and Encoder using logic gates.

APPARATUS REQUIRED:

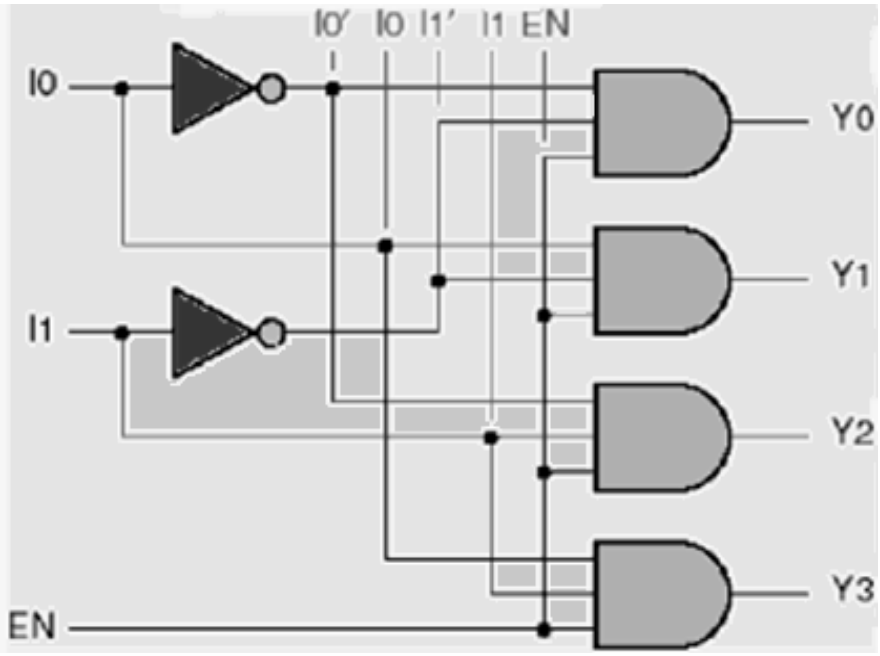
Sr.No.	Name of apparatus	Specification	Quantity
1	Encoder/decoder kit	Using logic gates	01
2	Patch cords	----------	As required

THEORY:

Decoder:

A Decoder is a multiple –input and multiple output combinational logic circuits which converts coded inputs into coded outputs, where the input and output coded are different.

Logic diagram of 2 to 4 Decoder



Procedure:

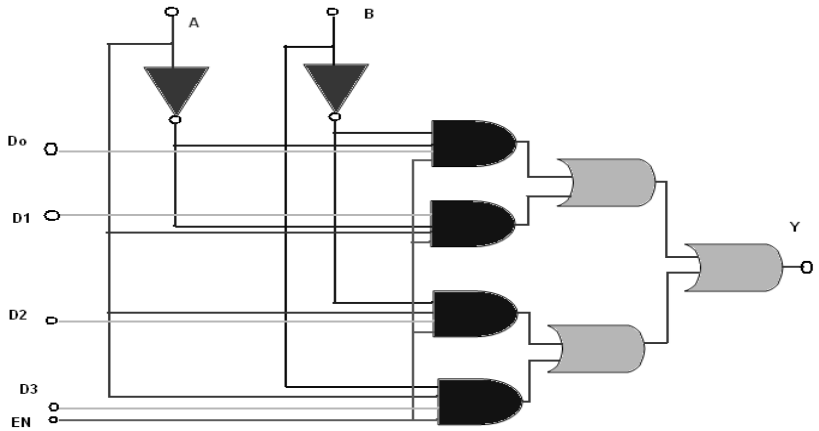
- Connect the supply from the trainer kit through patch cords, also connect circuit diagram as per circuit diagram.
- Give the input to A, B and EN through switches.
- Observe the output Y_o to Y_3 on the trainer kit through LEDs.
- For different combinations of inputs observe the outputs and match them with truth table.

Truth Table

Inputs			Outputs			
EN	A	B	Y_3	Y_2	Y_1	Y_o
1	X	X	0	0	0	0
0	0	0	0	0	0	1
0	0	1	0	0	1	0
0	1	0	0	1	0	0
0	1	1	1	0	0	0

Encoder:

An encoder is a combinations logic circuit. It is the reverse of a decoder function. It has 2^n input lines and n output lines. An encoder accepts an active level on one of its inputs representing a digit such as a decimal/octal digit and it convert to coded output.



Result: We have Implemented & verified of Decoder/Demultiplexer and Encoder using logic gates.